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APPLICATION

FOR

UNITED STATES LETTERS PATENT

Be it known that we, David Meltzer, of 268 Maloney Road, Wappingers Falls, New York, 12590, a citizen of the U.S.A., and Gregory Blum, of 53 Cunningham Dr., LaGrangeville, NY 12540, a citizen of the U.S.A., have invented new and useful improvements in:

A FREQUENCY/PHASE LOCKED LOOP CLOCK SYNTHESIZER USING AN ALL DIGITAL FREQUENCY DETECTOR AND AN ANALOG PHASE DETECTOR

of which the following is the specification

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Ann F. George

A FREQUENCY/PHASE LOCKED LOOP CLOCK SYNTHESIZER USING AN ALL DIGITAL FREQUENCY DETECTOR AND AN ANALOG PHASE DETECTOR

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RELATED APPLICATIONS

This application claims priority under 35 U.S.C. § 119(e) from application serial no. 60/459,854, filed April 1, 2003.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to the field of integrated frequency synthesizers and oscillators. Specifically, the present invention relates to the field of variable voltage oscillators implemented using low voltage digital CMOS processes.

Description of the Related Art

High speed Phase Locked Loops are used in modern communication systems for many purposes, including frequency synthesizing operations such as clock generation, data recovery, and retiming. Such frequency synthesizers are typically analog circuits, but to lower cost a trend in industry is to implement such circuits using low voltage digital CMOS processes.

Frequency synthesizers are typically voltage controlled, and thus suffer from signal headroom and scalability problems when implemented in low voltage digital CMOS processes. In spite of these problems, use of advanced submicron digital CMOS processes to implement analog clock generation and recovery continues to increase due to its benefit of significantly lower operating voltages.

As operating voltages are reduced, however, the amount of voltage range, or voltage headroom, available for these analog circuits is significantly reduced. As a result, the voltage range available for a frequency control and correction signal is greatly reduced requiring that the oscillator function within more rigid design parameters. Thus, this decreased headroom for analog circuits imposes a significant constraint on circuit design in high frequency clock synthesis.

Although, the corollary to this trend is the availability of complex digital functions in minimal area, it is well known that the integration of complex high

speed digital functions in close proximity to low headroom, high gain analog clock components gives rise to spurious frequencies and higher jitter components.

Thus, a need exists for a method of implementing analog circuits within a low voltage digital CMOS process with reduced jitter and expanded voltage head room.

OBJECTS OF THE INVENTION

The present invention is directed to solving these problems.

One object of the present invention is to provide an voltage controlled oscillator, VCO, suitable for integration in a low voltage digital CMOS process, in which the VCO's voltage head room is not much reduced from its rail-to-rail voltage range.

Another object of the present invention is to provide an analog VCO in a low voltage digital CMOS process with reduced jitter and greater frequency locking range.

It is still another object of the present invention to provide a simple method for implementing an analog VCO in a digital CMOS process without requiring modification of the CMOS process.

SUMMARY OF THE INVENTION

To achieve these objects, the present invention implements a frequency synthesizer having a dual loop structure including an analog loop and a digital loop to control a voltage controlled oscillator, VCO. The digital loop includes an all digital frequency difference detector (FDD), which controls the center frequency of the VCO. The analog loop includes an analog phase frequency detector (PFD) and charge pump, which adds phase coherence to the frequency controlled loop, thus eliminating any static frequency error. In effect, the analog loop reduces the noise of the digital logic and VCO, and the digital control provides frequency holdover and very low bandwidth. The bandwidth of the digital loop is made much smaller than the bandwidth of analog loop. Preferably, the bandwidth of the analog loop is at least 200 times greater than the bandwidth of the digital loop. This gross parametric difference is used in the design of the VCO to allow two separate control inputs, a first analog control input provided by the PFD within the analog loop and a second digital control signal provided by the FDD within the digital loop. Both control inputs function relatively independently of each other.

In a first embodiment of the present invention, the VCO is provided with two frequency adjusting mechanisms separately responsive to the first control input from the PFD and to the second control input from the FDD, respectively. The first frequency adjusting mechanism includes a varactor pair responsive to the first, analog control input from the PFD. The second frequency adjusting mechanism includes an array of capacitor/switch pairs, wherein the switches are each responsive to separate bit lines of digital signal bus conveying the second, digital control signal from the FDD. The switches conditionally couple and decouple their corresponding capacitor to and from said VCO circuit in accordance with the second control input.

The digital frequency difference detector includes an n-bit counter to count cycles of a reference frequency and an m-bit counter to count cycles of the oscillating output signal from the VCO, where m is greater than n. Both counters are reset, stopped, and started together in accordance with a control logic circuit.

Two memory cells, preferably implemented as latches, monitor the nth and (n+1)th bit within the m-bit counter and record when either of the nth or (n+1)th bit transition to a logic high. Both latches retain their recorded condition until they are reset by the control logic circuit irrespective of whether the nth or (n+1)th bit within the m-bit counter later transition back to a logic low while in the process of counting the cycles of VCO's output. Both counters are automatically stopped in response to the nth bit within the n-bit counter transitioning to a logic high. At this point, the current data contents of the m-bit counter, as well as the stored contents of the two memory cells are studied. A predetermined number of least significant bits (LSB's) within the m-bit counter are ignored to disregard any difference in the count of the n-bit counter and the m-bit counter due to relative phase differences between the VCO's output signal and the reference frequency signal. From the data content of the m-bit counter (excluding the predetermined number of LSB's) and the set conditions of the two memory cells, the control logic circuit determines if the VCO's output frequency is faster than, slower than, or locked to the reference frequency signal, and sends an appropriate second control signal to the VCO to compensate as required.

The architecture of the FDD provides an inherent low pass filtering operation for filtering the frequency difference between the reference frequency signal and the VCO's output signal. The bandwidth of the FDD's inherent low

pass filter is adjustable by increasing or decreasing the value of n in said n-bit counter and adjusting the increment/decrement digital step size of the second control signal sent to the VCO.

Other objects and attainments together with a fuller understanding of the invention will become apparent and appreciated by referring to the following description and claims taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a frequency synthesizer in accord with a first embodiment of the present invention.

Fig. 2 is a first implementation of a voltage controlled oscillator with the present invention.

Fig. 3 is a block diagram of a digital frequency detector in accord with the present invention.

Fig. 4 is a linearized model of a frequency synthesizer in accord with the present invention.

Fig. 5 is a second embodiment of a frequency synthesizer in accord with the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention are described below with reference to the accompanying figures.

With reference to Fig. 1, a frequency synthesizer 10, or clock synthesizer, in accord with the present invention includes a variable oscillator 11, preferably a voltage controlled oscillator (VCO), having a first control input 11a and second control input 11b. VCO 11 produces an oscillator output signal whose frequency is dependent on both its first 11a and second 11b control inputs.

Frequency synthesizer 10 also includes an analog phase detector 13 and a digital frequency difference detector (FDD) 15. Preferably, analog phase detector 13, which is sometimes referred to as phase frequency detector, PFD, includes a charge pump, not separately shown. Analog phase detector 13 has first 13a and second 13b phase-detection inputs and is effective for producing a first control signal representative of the phase difference of signals applied to its first 13a and second 13b phase-detection inputs. Digital frequency

difference detector 15 has first 15a and second 15b frequency-detection inputs, and is effective for producing second control signal representative of the frequency difference of signals applied to its first 15a and second 15b frequency-detection inputs. The first and second control signals from analog phase detector 13 and digital frequency difference detector 15 are coupled to the first 11a and second 11b control inputs of VCO 11, respectively. Preferably, the first control signal of analog phase detector 13 is couple to the first control input 11a of VCO 11 via an analog loop filter 27.

It is to be understood that the first control signal output from analog phase detector, or analog phase/frequency detector, 13 is an analog signal, and it may represent a varying phase difference by a proportionally varying signal intensity. It is also to be understood that the second control signal output from digital frequency difference detector 15 is a digital signal, which outputs onto a single conductive line or onto a signal bus, and has a digital value indicative of a frequency difference.

An input node 10a of frequency synthesizer 10 receives a reference frequency signal, which in the present case is embodied by a reference clock input signal. If desired, the reference clock input signal may be applied directly to first phase-detection input 13a and first frequency-detection input 15a, but it is preferred that the frequency of the reference clock input signal first be stepped down by passing it through a first frequency divider 21. The output of this Reference Clock Synchronous Divider 21 is applied to analog phase detector 13 and digital frequency difference detector 15. It is to be understood that use of a frequency divider is a design choice for reducing design complexity, and not critical to the invention.

In a similar manner, the oscillator output signal from VCO 11 may be fed back directly to second phase-detection input 13b and second frequency-detection input 15b, but it is preferred that its frequency also first be stepped down by passing it through a second frequency divider, i.e. VCO Synchronous divider 23. In the present case the oscillator output signal is passed through another frequency divider, Output Synchronous Divider 25, to produce the Synchronized Clock Output signal of frequency synthesizer 10.

In this manner, frequency synthesizer 10 incorporates a conventional analog Phase Lock Loop (PLL) structure consisting of the path from analog phase detector 13 to VCO 11 and back to analog phase detector 13. The present invention further adds a second, digital loop to the conventional PLL structure. The digital loop is defined by the path from digital frequency difference detector

15 to VCO 11 and back to frequency difference detector 15. Preferably, the bandwidth of the digital loop is made much smaller than the bandwidth of analog loop. In the present embodiment, the bandwidth of the analog loop is at least 200 times greater than the bandwidth of the digital loop. This gross parametric difference is used in the design of VCO 11 to allow two separate control inputs, one from the analog loop and one from the digital loop.

Thus, the present invention implements a dual loop controlled frequency synthesizer, with one loop being a digital loop and the other being an analog loop. In the present first embodiment, the digital loop includes the all digital frequency detector 15, which controls the center frequency of VCO 11 and thereby reduces the voltage swing needed for the first control signal from the analog loop and increases the pulling range of the VCO. The analog loop, which includes low gain, analog phase detector/charge pump 13, adds phase coherence to the frequency controlled loop, thus eliminating any static frequency error. In effect, the analog loop reduces the noise of the digital logic and VCO 11. The digital control provides frequency holdover and very low bandwidth.

As specified above, the second control signal, which is output from digital frequency difference detector, FDD, 15 may be placed onto a signal bus that provides digital control for VCO 11. With reference to Fig. 2, a sample implementation of VCO 11 suitable for receiving a digital control bus 31 from FDD 15 as its second control input 11b is shown.

The present embodiment uses a current limited, cross-coupled inverter pair, LC, CMOS oscillator with its frequency controlled by first control input 13a, carrying analog signal VCTL from analog phase detector 13, and by second control input 13b carrying the digital control bus signal from FDD 15. First inverter INV1 (consisting of PMOS transistor P1 and NMOS transistor N1) is cross-coupled with second inverter INV2 (consisting of PMOS transistor P2 and NMOS transistor N2). The current through inverters INV1 and INV is limited by a current source, i.e. a current tail I1, consisting of NMOS transistor N3 and set by a bias signal Vbias. An inductor L1 is coupled across the outputs of INV1 and INV2. The frequency of VCO 11 is adjusted by adjusting two separate capacitive parameters.

The first capacitive parameter is embodied by a varactor diode pair, D1 and D2, which vary their capacitive value in accordance with control voltage VCTL. The varactor diode pair D1/D2 is coupled in parallel to inductor L1 to form an LC tank.

The second capacitive parameter is embodied by an array of capacitors Ci to Cp switched in and out of the oscillator circuit by corresponding transistors Mi to Mp according to the value contained on a corresponding bit line bi to bp of the digital control bus 31. Thus, the digital control signal from FDD 15 selectively couples and decouples specific capacitors of array Ci-Cp to and from the oscillator circuit. In the present embodiment, the array of capacitors Ci-Cp is returned to the drain of the tail current transistor N3, i.e. capacitors Ci to Cp are selectively coupled from the outputs of INV1 and INV2 to the source electrode of transistor N3. Alternatively, the array of transistor/capacitors pairs Mi/Ci to Mp/Cp could also be returned to ground. This would increase the tuning range, but might increase noise in the oscillator.

FDD 15 of Fig. 1 may be implemented in different ways. For example, FDD 15 could be of the type that directly determines the frequency of the reference clock and generates a digital control value needed to set the array of capacitors and control switches Mi/Ci to Mp/Cp. However, this requires the equivalent of a set of coefficients correlating each digital value to a frequency of oscillation of VCO 11, which are very dependent on manufacturing process, voltage, and temperature variations. The presently preferred FDD embodiment therefore takes a different approach, and generates only a frequency difference indicator, to increment or decrement the capacitance value of the array of capacitors Ci to Cp.

With reference to Fig. 3, a block structure of digital frequency difference detector, FDD 15, in accord with the present invention preferably includes two binary ripple counters 41 and 43, both having reset inputs controlled by a sequential state machine 45, which is part of a control logic circuit for coordinating the operation of the various logic blocks making up FDD 15. Ripple counters 41 and 43 increment on one edge (either the rising or falling logic edge) of signals applied to their respective inputs. The reference frequency signal applied at input 10a of Fig. 1 (or a stepped down representation of it supplied from frequency divider 21) is coupled to the Reference Clock Input of first AND gate 47. First AND gate 47 functions as a masking gate to selectively allow the reference frequency signal applied to its Reference Clock Input to pass through and be applied to the input of ripple counter 41 as determined by RUN/STOP control signal 51 from sequential state machine 45, or to selectively halt the reference frequency signal and prevent the incrementing of ripple counter 41. Similarly, the oscillator output signal from VCO 11 (or a stepped down representation of it supplied from frequency

divider 23) is coupled to a VCO Clock input of a second AND gate 49, which functions as a second masking gate to selectively allow the oscillator output signal to pass through and be applied to the input of ripple counter 43 as determined by RUN/STOP control signal 51, or to selectively halt the oscillator output signal and prevent the incrementing of ripple counter 43.

In this manner, ripple counters 41 and 43 respectively count cycles of the reference frequency signal (at the Reference Clock Input node) and the oscillator output signal (at the VCO Clock input node). Counter 41 is a binary counter of n bits, and counter 43 is binary counter of m bits, where m is greater than, or equal to, n+1. Two one-bit latches, 53 and 55, functions as memory cells to monitor the nth and (n+1)th bits among the m bits of counter 43, and to remember any overflows of the reference count through bit n and n+1. Latches 53 and 55 record when the nth bit and/or the (n+1)th bit of counter 43 transition from a logic low 0 to a logic 1 (assuming that counter 43 is an up-counter).

Preferably, each rising edge of a signal at the Reference Clock Input causes counter 41 to increment its count, and each rising edge of a signal at the VCO Clock input causes the counter 43 to increment its count. Whenever the nth bit of counter 43 is set, i.e. transitions to a logic high, due to an increment-count operation, latch 53 is set and remains set until it is cleared by sequential state machine 45, irrespective of whether the nth bit later transition back to a logic low due to continued counting by counter 43. Whenever the (n+1)th bit of counter 43 is set, i.e. transitions to a logic high, due to an increment-count operation, latch 55 is set and remains set until it is cleared by sequential state machine 45.

The count value of counter 41 is monitored by a combinational logic network 57, which conveys the information to sequential state machine 45. Specifically, combinational logic network 57 monitors the nth and (n-1)th bits of counter 41. When the nth bit of counter 41 is set (i.e. transitions to a logic high) and its n-1 bit is reset (i.e. transitions back to a logic low), indicating an overflow out of bit n-1 into bit n, sequential state machine 45 issues the RUN/STOP signal to masking gates 47 and 49 to stop the increment-count operations of both counters 41 and 43. This freezes the count contents of both counters 41 and 43.

When counter 41 is stopped, its count contents and the set conditions of latches 53 and 55 are examined and used to determine the relative frequency of the reference frequency signal and oscillator output signal, as observed at the

Reference Clock Input and VCO Clock Input, respectively. In the present example, this determination is made by a second combinational logic network 61. It is to be understood that sequential state machine 45, first combinational logic circuit 57 and second combinational logic circuit 61 may be integral parts of a general control logic circuit of FDD 15. If combinational logic network 61 determines that the frequency of the oscillator output signal is higher than the frequency of the reference frequency signal, then it will transmit signal FAST to a first latch L1. If combinational logic network 61 determines that the frequency of the oscillator output signal is lower than that of the reference frequency signal, then it will transmit signal SLOW to second latch L2. If combinational logic network 61 determines that the frequency of the oscillator output is locked to that of the reference frequency signal, then it transmit signal LOCK to third latch L3. Latches L1, L2 and L3 latch in the transmitted signal from combinational logic network 61 in response to command signal SAMPLE issued from sequential state machine 45.

The frequency of the oscillator output signal from VCO 11 is determined to be less than the reference frequency signal if both latches 53 and 55 are not set. Latch 55 must also be off to ensure that more than one complete cycle of counter 43 has not occurred.

The frequency of the oscillator output signal from VCO 11 is determined to be greater than the frequency of the reference frequency signal if more count operations took place in counter 43 than in counter 41. This is the case if either of two conditions are met. The frequency of the oscillator output signal is greater than that of the reference frequency signal if both latches 53 and 55 are set, indicating an overflow out of bit n of counter 43, or if latch 55 is set and there are any logic high bits in stages 2 through n of counter 43. The least significant bit (LSB) (i.e. stage 1) is not checked because there can be a 1 bit difference in the count due to relative phase differences between the oscillator output signal and the reference frequency signal. In the present case, only stage 1, i.e. the lowest value bit, is ignored to account for this possible phase difference. But other number of least significant bits (i.e. such as stages 1 and 2) may be ignored to account for this possible phase difference.

Alternatively, if latch 53 is set and latch 55 is not set, and if there are no logic highs set in any of the bits below the nth bit of counter 43 (excluding the LSB bits that are ignored due to possible phase difference), then the oscillator clock signal and the reference frequency signal are determined to be locked.

After this determination is made, the counters 41 and 43 can be reset and a new measurement cycle can begin. The measurement of the relative frequency of the oscillator output signal and the reference frequency signal stored in latches L1, L2, and L3 indicating either fast, slow or locked are conveyed to an up/down counter 65. Sequential state machine 45 then generates a clock signal for up/down counter 65 to respond to the latched conditions.

In the present embodiment, each bit of counter 65 controls a corresponding one of switch transistors Mi to Mp of Fig.2. The measurement is used to increment or decrement up/down counter 65 to correct the center frequency of VCO 11. The direction of change for up/down counter 65 is dependent on the pulling curve slope of VCO 11. For the exemplary oscillator structure of Fig. 2, which has a negative slope, the counter is decremented if the measurement indicates that the frequency of the oscillator output signal of VCO 11 is slower than that of the reference frequency signal.

The above description shows that a measurement is taken every 2**(n-1) periods of the Reference Clock Input. This is an inherent low pass filtering operation of the frequency difference value. The actual time constant of the response of this filter is dependent on the Reference Clock Input, i.e. the reference frequency signal [which determines the measurement interval], the frequency difference and the number of bits in up/down counter 65. The filter bandwidth can be adjusted by increasing or decreasing the number of bits in the counter and the increment/decrement step size of the up/down counter.

The accuracy of the frequency difference measurement can be adjusted by changing the number of bits in counters 41 and 43, but in general it is unnecessary to have many more bits than there are bits in up/down counter 65, i.e. capacitance steps in the oscillator. Changing the number of bits in counters 41 and 43 also changes the measurement interval. There is an inverse relationship between accuracy and filtering bandwidth. Increasing the measurement interval also increases the acquisition time of the loop. Since the measurement interval is determined by the transitions of the Reference Clock Input, loss of the Reference Clock Input can provide an automatic holdover for VCO 11. In the dual loop system of Fig. 1, a signal must be generated indicating loss of reference to turn off the analog charge pump if the holdover is desired.

With reference to Fig. 4, a simplified linearized model of the dual loop frequency synthesizer system of the present invention has an input frequency

Fin applied to a first input of a frequency difference node 81, and is also converted to relative phase by block 83 that is applied to a first input of a phase difference node 85. The output from a VCO 87 of gain Kv is applied to the second input of frequency difference node 81. The frequency difference is sampled and converted to voltage with gain Kfdd by stages 91 and 93. The output frequency from VCO 87 is converted to a relative phase by block 95 and applied to the second input of phase difference node 85. The phase difference is converted to a voltage with gain $K\phi$ by stage 97, which may comprise the phase detector and charge pump of Fig. 1. The output of stage 97 is filtered with transfer function R(s) at stage 99 and summed at summation node 101 with the frequency difference detector output from stage 93. The output of summation node 101 controls VCO 87.

As shown, the frequency output 103 of VCO 87 closes the digital frequency difference loop and its phase output 105 closes the analog phase detector loop. This simple model may be used on a circuit simulator to investigate the effects of component bandwidths including the VCO modulation bandwidth, filter characteristics, pump currents, etc. Simulations on a Cadence SPECTRE simulator were used to select the values of components in an experimental test chip. Applying a frequency step input to this model showed that each frequency correction measurement is a time delayed frequency step which causes the analog loop to respond. Improper choice of measurement intervals, filters, and pump current can cause the two corrections to oscillate in opposite directions. However, when the measurement interval for the digital frequency detector, i.e. the frequency sampling interval, is large compared to the bandwidth of the analog phase detection loop, the output Vf of the frequency detector can be regarded as a fixed value while the analog loop responds. The frequency transfer function then becomes the sum of two terms $[sKvVf/(s+K\phi R(s))] + [KvR(s)Fi/(s+KfR(s))]$, a fixed value contributed by the FDD and a variable term for the analog correction. This implies that the gain $K\phi R$ must be kept low in order for the frequency detector loop to dominate.

A chip was built using a 0.18 μm digital logic process to test this proposed frequency synthesizer architecture. Two changes were made to the VCO structure of Fig. 2 to simplify the oscillator design and reduce the size of the required inductor. The first change was the elimination of the tail current source transistor N3. This reduced the frequency of oscillation for a constant sized inductor due to the increased capacitance to ground of the gain transistors. This also increased the noise of the oscillator. However, the

increased gain of the cross-coupled inverters over a current limited oscillator allowed operation at a reduced voltage with increased filtering in the supply. The second major change was the use of a 10 bit Digital to Analog Converter (DAC 113 in Fig. 5) and a voltage summing amplifier (115 in Fig. 5) to generate an analog control voltage for the oscillator and eliminate the array of transistor/capacitors Mi/Ci to Mp/Cp (from Fig. 2). This was a pure design choice that allowed a simplified layout of the oscillator for the test chip at the expense of reduced pulling range and increased noise. A diagram of the test chip as built is shown in Fig. 5, including the alternate embodiment of VCO 11.

With reference to Fig. 5, all elements similar to those of Figs. 1-4 have similar reference characters and are described above. In the presently preferred embodiment, the input reference frequency signal is implemented as an AC coupled LVDS style signal with a 100 ohm R resistor differential termination. As it is known in the art, low voltage difference signals (LVDS) convey information using a differential signaling technique wherein a first signal line 135a carries the true logic of a signal and a second signal line 135b carries its logic complement. In the present case, the differential input signals 135a/135b constituting the reference frequency signal are capacitively coupled to differential receiver 111 by means of two capacitors Cin1 and Cin2. The differential output driver 121 uses a similar drive scheme with a preferred 5 mA current drive.

In the present embodiment, differential receiver 111 converts the differential reference frequency signal of inputs 135a and 135b into a single-ended signal applied to input 10a of frequency divider 21. This is purely a design choice to simplify the comparison of the embodiment of Fig. 5 with that of Fig. 1. It is to be understood that the embodiments of Figs. 1 and 5 can be used to process a differential input signal without converting it to a single-ended signal by using appropriate differential mode structures for their circuit blocks.

As in the previous case of Fig. 1, the single-ended reference frequency signal of Fig. 5 is applied to optional frequency divider 21 whose output is applied to both analog phase frequency detector 13 (with optional charge pump) and to digital frequency detector 15. Also like in the embodiment of Fig. 1, the output from the analog phase detector 13 subjected to a loop filter 27. However in present case, loop filter 27 on the charge pump output is made external to the chip for ease of construction, and is implemented as a standard second order filter consisting of capacitors Cf1, Cf2, and resistor Rf1. In the

present case, the parasitic capacitance of an ESD protection circuit, not sown, was used as the second capacitor in filter 27 with a value of 3 pF.

The three synchronous dividers 21, 23 and 25 were implemented in a shift register style rather than as binary dividers in order to generate specific frequencies. The synchronous dividers 21, 23 and 25 were built in two serial sections, the first capable of producing nominal 50% duty cycle pulses at all integer division ratios between 1 and 8 which feeds the second stage capable of producing all integer division ratios between 1 and 17. In the results reported here the second stage is always set to divide by 1.

As explained above, the output of digital FDD 15 is converted to an analog representation by digital-to-analog converter, DAC 113. The outputs from digital FDD 15 and analog PFD 13 are summed by summer circuit 115, which produces a control signal 131 to adjust the frequency of VCO 11 accordingly.

Also as explained above, VCO 11 is simplified in the present embodiment and consists only of cross-coupled inverters INV1 and INV2, varactor pair D1/D2, and inductor L1.

In the constructed test chip, the oscillator inductor was measured at 3.1 nH. Table I shows some of the characteristics of the experimental chip. The chip was operated at one voltage with a separate input pin for the VCO Vdd. The power was measured while the synthesizer was locked at 1.1GHz. Note that the summing amplifier passband was only 3MHz and so represented an upper limit on the open loop response of the analog phase detector loop. The size of the frequency counters determined a measurement interval of 131 μsec, corresponding to a high frequency response of 7.6KHz for a minimum frequency step.

TABLE I
EXPERIMENTAL CHIP CHARACTERISTICS

Process	.18μm digital CMOS	
Total chip	size 2.8 x 2.8 μm	
Vdd	1.8V	
Power [at 1.1GHz]	Total	100.8 mw
	VCO	37 mw
	DigitalFDD	200μw
VCO Frequency	1.02 GHz min	1.27 GHz max
FDD characteristics	area	.11mm[272x403μm]
	cycle counters	17 bits

	frequency	10 bits
	dead band	1 LSB
Analog PFD/CP	pump current	50 μa
Summing Amplifier	Bandwidth	3MHz

Measurements were taken to determine the effect of operation of both loops simultaneously on lock range and jitter. Lock range for operation with the frequency loop alone was defined to be the region of stable loop operation. This is when the frequency difference detector indicated lock and only a difference corresponding to 1 LSB in the frequency counter was observed. This definition was used since there was no phase coherence with the input. When both loops were operating simultaneously, the region of lock was defined as the frequency range for coherence with the input. Jitter was measured with an Agilent® 86100A Digital Communications Analyzer which combines deterministic and random jitter into one measured number.

Examination of the spectrum of the synthesized clock showed a significant number of spurious frequency components due to the switching of the frequency counters and cross products of these frequencies and the reference clock frequency. This was most probably due to the use of a single supply for both analog and digital functions and the relatively poor decoupling of the digital noise. This contributed to the deterministic jitter but could not be separated in the measured number. The low bandwidth of the summing amplifier limited the ability of the analog loop in combined operating mode from reducing this jitter. Nevertheless, the combined loop operation showed a larger lock range, as expected, and a reduction of jitter due to the analog loop.

Table II shows the lock range and jitter as a function of closed loop gain variation caused by changing the feedback divider ratio. The loop filter bandwidth for the analog output was maintained constant at 1.6MHz as was the pump current for purposes of comparison. The lower value of the frequency in the lock range was always between 1.02 to 1.03GHz. This shows that operation of both loops together significantly improves the lock range and both RMS and Peak-to-Peak jitter significantly. The low bandwidth of the digital frequency detector coupled with the low gain of the wider bandwidth analog loop should improve the jitter transfer characteristic over a wide band analog only loop.

TABLE II
LOCK RANGE AND JITTER

Gain	FDD only			FDD + Analog PFD		
	Lock	jitter	jitter	Lock	jitter	jitter

	Range MHz	RMS psec	P-P psec	Range MHz	RMS psec	P-P psec
1	35	5.8	16	6	3.8	15.6
2	170	4.2	8.5	155	2.5	6.8
3	182	4.2	8	209	3.7	6.9
4	184	4	8.2	246	3.2	6.6
5	180	3.8	21	196	1.5	6.6

In the above described test chip, a clock synthesizer using a digital frequency difference detector and an analog phase detector/charge pump operating simultaneously was constructed. The digital frequency difference detector occupies a negligible area and consumes very little power. Due to its all digital nature it offers the possibility of scaling better with lithography than a purely analog design. Even with unoptimized filtering, the test chip showed that the small analog phase detector/charge pump significantly improved the jitter characteristics of the frequency controlled loop without sacrificing any lock range.

The present invention has been described in connection with various preferred embodiments thereof with reference to the accompanying drawings. However, various changes and modifications will be apparent to those skilled in the art based on the foregoing description. Such changes and modifications are intended to be included within the scope of the present invention to the extent they fall within the scope of the appended claims.